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Application Note

INTERFACE TECHNIQUES BETWEEN INDUSTRIAL LOGIC AND POWER DEVICES

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This application note presents worst case design approaches to illustrate the methods of interfacing McMOS and MHTL logic to various power load levels, both ac and dc. Interface devices vary from small-signal transistors to power transistors and thyristors, using direct coupling/level translation and optoelectronic coupling techniques.

MOTOROLA *Semiconductor Products Inc.*

Interface Techniques Between Industrial Logic and Power Devices

INTRODUCTION

A question often asked by logic designers is "How does one interface between logic I.C. outputs and loads requiring power gain?" It is a straight forward procedure when interfacing between logic outputs and logic inputs, knowing the input and output loading factors, device threshold characteristics and power requirements. However, more information is needed for interfacing with loads requiring additional power.

This application note illustrates how to interface between logic and power devices by interpreting from the data sheet the output parameters of the logic devices, defining the load requirements and, thus, characterizing the interface element.

The logic families that are illustrated, McMOS and MHTL, are primarily those used in industrial environments. However, any logic (MTTL, MRTL, MDTL and MECL) can be readily used simply by translating its output characteristics, using the illustrated design criteria, to the specified conditions.

The High Threshold Logic (HTL) chosen to illustrate these interface techniques are of both active and passive outputs with examples shown using both high and low level logic output to activate the load. The CMOS examples also illustrate both logic levels for load activation.

The power devices described cover the range from small-signal transistors to power transistors and thyristors, predicated on the power level and types of load, ac or dc, to be controlled. The described interfacing between the logic output and the power device is generally accomplished by direct coupling and level translations. Other techniques, such as optoelectronic coupling, are also illustrated.

Another interface approach depicted is the use of higher current I.C. drivers (25 to 300 mA) to directly interface with these power level loads, of which several examples of McMOS, MHTL and MTTL are shown.

CURRENT SINK/SOURCE CONSIDERATIONS

The two logic families that are extremely well-suited for most industrial high noise environments are the MHTL – Motorola High Threshold Logic – and McMOS – Motorola Complementary MOS. Both families have large noise margins, typical 5 V for MHTL and 45% of V_{DD} for McMOS. For this reason, most of the design criteria established will be tailored to these families, but they can be readily translated to any logic family, i.e., MTTL, MDTL, etc.

MHTL

When interfacing between logic outputs and logic inputs, the circuit designer needs only to establish what are the input and output loading factors – the source and sink current capability of the device. As an example, the MC670, a triple 3-input NAND gate (passive pull-up) of the HTL family, has an input loading factor of one and an output loading factor of ten. Additionally, the data sheets states the following:

Output voltage V_{OL} = 1.5 V max at I_{OL} = 12 mA

V_{OH} = 12.5 V min at I_{OH} = 30 μA

Reverse Current I_R = 2 μA max at V_R = 16 V

I_F = -1.2 mA max at V_F = 1.5 V

Thus, when driving ten loads, the device has a sink current capability of 10 I_F equal to 12mA with the low level output voltage V_{OL} guaranteed to be less than 1.5Vmax (typically $V_{CE(sat)} \cong 0.2V$). Similarily, when sourcing ten loads, the specified minimum output voltage will exceed 12.5V at a source current at 30μA, a value somewhat higher than the ten reverse current loads (10 x 2 = 20μA). This does not imply that the device can only source 30μA. It only states the device is guaranteed to have a high level, minimum output voltage of 12.5V at that 30μA. Normally, when driving other logic gates, the high level (one) driver output need only reverse bias the input diodes (or emitter-base junctions) and source the specified leakage current.

However, when driving other than logic devices, namely discrete circuits, the following criteria will suffice. Figure 1(a) shows the schematic of one 3-input gate of the triple NAND gate, the "passive pull-up" MC670; however, for this illustration, any passive pull-up gate (or logic function) could be used. When load resistor R_{L1} is connected as illustrated, the sink current is dictated by the simple equation $I_{sink} = \frac{V_{CC} - V_{OL}}{R_{L1}}$ and the maximum specified sink current of 12mA, which, in turn, is limited to minimum h_{FE} of the output transistor (Q2).

With the output at the logic one level (Q_2 not conducting), the source current is simply expressed by $I_{source} \approx \frac{15V}{15\ k + R_{L2}}$. The limiting value of source

McMOS, MHTL, MTTL, MRTL, MDTL, MECL are trademarks of Motorola Inc.

current would be when R_{L_2} is zero (the output short-circuited) and would be $\frac{15V}{15\,k}$ or 1mA. The specified short-circuit current I_{SC} is 1.5mA and is due to the -33% resistor tolerance of the 15 k Q_2 collector resistor [67% (15 k) = 10 k].

Thus, when directly interfacing with the base-emitter load of an NPN transistor, the nominal source current (or base current for that transistor) would be $\frac{15V - .7V}{15\,k} \cong$ 1mA for the passive pull-up gate.

The sink current limitations of the HTL "active pull-up" gate (Fig. 1(b)) is identical to that of the passive pull-up and is also specified as 12mA. This figure shows one 2-input NAND gate of the quad MC672 but the discussion is applicable to any active pull-up device. When the output is low (logic zero), transistor Q_3 is off and the sink current is expressed as

$$I_{sink} = \frac{V_{CC} - V_{OL}}{R_{L_1}} \text{ where } V_{OL} = V_{CE(sat)} + V_{D_3} \approx 1.5V \text{ max}$$

The sourcing capability of an active pull-up gate is quite different from that of the passive pull-up case and is shown in Figure 1(c). When the gate output is high (logic one), Q_2 is cut-off and the circuit operates as an emitter-follower. The input impedance Z_{in} of that circuit results in a base voltage V_B and thus an output voltage V_{OH}, as shown.

$$V_{OH} = \frac{15(h_{FE}R_{L_2})}{h_{FE}R_{L_2} + 15\,k} - V_{BE}$$

For worst case design, h_{FE} min can be assumed to be ten.

For a particular sourced load, the high level output voltage can be readily calculated. The limiting source current occurs when the load is zero (output short-circuited) or simply, the emitter current resulting from the common-emitter configuration.

$$I_{source(max)} = I_E \cong \frac{V_{CC} - V_{CE(sat)Q3}}{R_C} = \frac{15 - .2}{1.5\,k} \cong 10mA$$

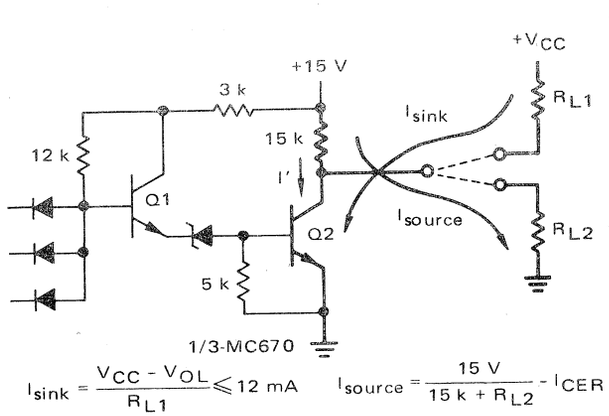


Figure 1a — Passive Pull-Up HTL Gate

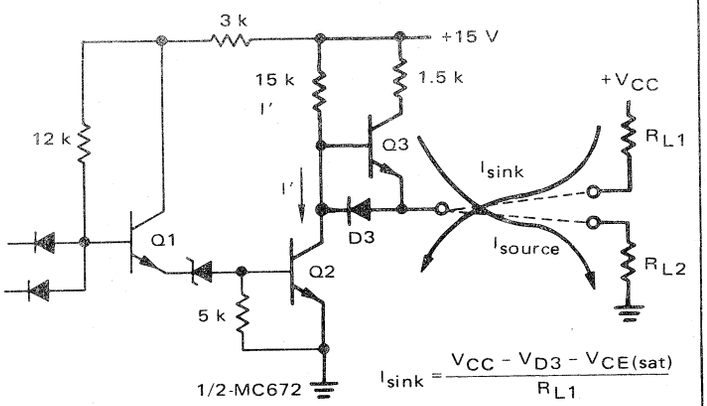


Figure 1b — Active Pull-Up HTL Gate

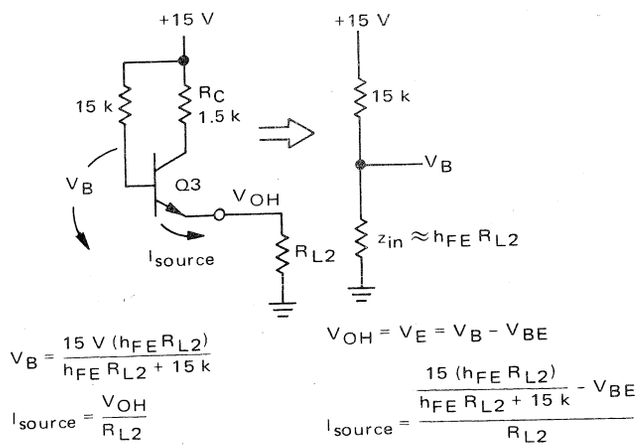


Figure 1c — Active Pull-Up Source Current Derivation

FIGURE 1 — SINKING/SOURCING OF MHTL GATES

The specified short-circuit current is 15mA maximum to take into account the tolerance variation of the collector limiting resistor R_C equal to 1.5 k.

When the output is directly coupled to an NPN common-emitter base-emitter junction, the source current will be nearly that of the short circuit current and will be

$$I_{source} \approx \frac{15 - .2 - .7}{1.5\ k} \approx 9.4mA.$$

However, the high level output will be clamped to the base-emitter voltage drop of the load transistor. By resistive coupling to the load, the high level output voltage V_{OH} can be maintained at a higher voltage level, if desired, dictated by the size of the coupling resistor and the base current requirements of the load transistor.

By extension, any type of load can be interfaced; the only criteria is that the sink or source current requirements of the load be within the capability of the logic device. However, to interface with larger loads requires power amplification, of which several examples will be illustrated later in this application note.

McMOS

The other popular logic family for industrial applications is the McMOS product line, the Complementary Metal Oxide Semiconductor devices, of which a schematic of a typical inverter is shown in Figure 2(a). To implement NOR and NAND gates from this configuration requires simply connecting these inverters in various series, parallel combinations.

The inverter consists of a P-channel MOS device connected in series with an N-channel device (drain-to-drain) with the gates tied together and driven from a common signal – hence, the name CMOS (Complementary MOS). When the input signal goes positive (+V), the P-channel device is essentially OFF and conducts only I_{DSS} (picoamperes). The N-channel unit is forward biased but since only I_{DSS} is available from the P-channel device, V_{DS} is very low. Conversely, when the input goes low (zero), the P-channel device is turned fully ON, the N-channel device is off, and the output will be very near +V. Since the current (without a load) is extremely small, the device dissipates almost no power in either stable state; the only dissipated power of consequence occurs during the switching transistions. Due to the extremely high input impedance of this CMOS device, it has the capability of interfacing with many CMOS gates, the fanout being greater than 50.

However, when interfacing with other loads, the CMOS gate is current limited mainly by its channel resistance and, to a second order effect, by its forward transadmittance. The dc resistance between drain and source when the device is turned on is generally labeled "ON resistance, R_{ON}" or $r_{DS(on)}$.

The equivalent circuits for sinking and sourcing current into an external load is shown in Figures 2(b) and 2(c). Normally, when interfacing CMOS to CMOS, because of the extremely small load currents the logic outputs will be very near their absolute maximum states (V_I or 0.0V). With other types of loads, the current and the resulting output voltage is dictated by the simple voltage divider of R_{ON} and the load resistor R_L where R_{ON} is the total series and/or parallel resistance of the devices comprising the NOR or NAND function.

An illustration or the sink/source currents at various supply voltages with the specified logic level outputs is shown in Table I. From this information, the ON resistance can be extrapolated for worst case design.

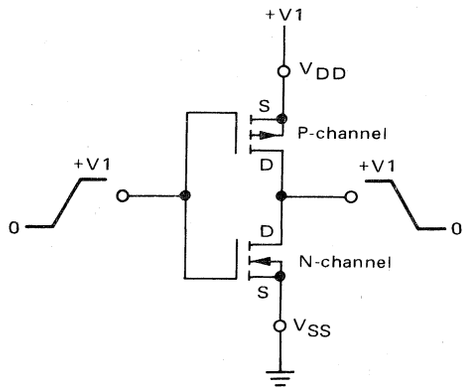
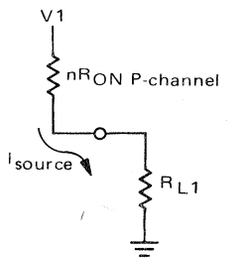


Figure 2a – CMOS Inverter

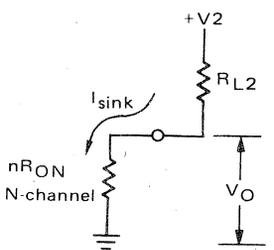


$$I_{source} = \frac{V1}{nR_{ONP} + R_{L1}}$$

$$V_O = \frac{V1\,R_{L1}}{nR_{ON\,P} + R_{L1}}$$

Where n = number of devices in series/parallel combinations of the NOR or NAND functions.

Figure 2b – Sourcing Current



$$I_{sink} = \frac{V2}{R_{L2} + nR\,ON_N}$$

$$V_O = V2 - \frac{V2\,R_{L2}}{R_{L2} + nR\,ON_N}$$

Figure 2c – Sinking Current

FIGURE 2 – CMOS SOURCE/SINK CAPABILITIES

TABLE 1 – Source/Sink Characteristics

Characteristic	Symbol	V_{DD} Vdc	AL Series Min	AL Series Typ	AL Series Max	CL/CP Series Min	CL/CP Series Typ	CL/CP Series Max	Unit
Output Drive Current									
P-Channel (I_{source})	I_{OH}								mA
(V_{OH} = 2.5 Vdc)		5.0	-0.5	-1.7	–	-0.2	-1.7	–	dc
(V_{OH} = 9.5 Vdc)		10	-0.5	-0.9	–	-0.2	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	–	-3.5	–	–	-3.5	–	
N-Channel (I_{sink})	I_{OL}								mA
(V_{OL} = 0.4 Vdc)		5.0	0.4	0.78	–	0.2	0.78	–	dc
(V_{OL} = 0.5 Vdc)		10	0.9	2.0	–	0.5	2.0	–	
(V_{OL} = 1.5 Vdc)		15	–	7.8	–	–	7.8	–	

As an example, for the CL/CP series with guarantees of:

$$V_{DD} = 10V$$

$$V_{OH} = 9.5V$$

and the source current $I_{OH(min)} = -0.2mA$, the maximum R_{ON} would be

$$R_{ON(max)} = \frac{V_{DD} - V_{OH}}{I_{OH(min)}} = \frac{10-9.5}{0.2} = 2.5\ k$$

Similarily, for the sink current condition, also at 10V, with $I_{OL(min)} = 0.5$ mA.

$$R_{ON(max)} = \frac{V_{OL} - V_{SS}}{I_{OL(min)}} = \frac{0.5-0}{0.5} = 1\ k.$$

Continuing these calculations for the other conditions, the maximum ON resistances can be approximated as shown in Table 2. It is apparent from this table that the ON resistance decreases with increasing supply voltage.

Although the minimum currents are not shown on the data sheet for the 15V case, the maximum ON resistance can be no greater than for the 10V example and can therefore be assumed for worst case approximation to be 1 k and 2.5 k for sink and source current cases respectively.

The sourcing ON resistance is greater than the sinking case due to the difference in carrier mobilities of the two channel types; N-material has about three times greater mobility than P-types and therefore, lower ON resistance. To partially compensate for this mobility factor, the P-channel MOS exhibits a larger geometry to reduce resistance.

Generally, for most CMOS devices, the maximum current is limited to 10mA. This is illustrated in the gate characteristic curves of the McMOS family data sheet for the 5V and 10V power supplies; the leveling off of the curves is due to the finite forward transadmittance y_{fs} of CMOS. With a 15V supply, the device is capable of supplying greater than 10mA but should be limited to that current to avoid exceeding the reliable limits of the unit metallization.

Since the lower supply voltage examples are effectively current limited, the CMOS outputs can be short-circuited and thus can directly drive transistor or diode junctions. The 15V circuit, however, must be current limited to 10mA by using a limiting series resistor with the load. The logic devices have now been defined as far as their current drive capabilities. What remains is to specify the load and determine the power gain required to interface with this load.

LOAD CHARACTERISTICS

Loads can be resistive, reactive and linear, or non-linear. With linear resistive loads (those loads that do not change resistance with power or time), the determination of the required power gain is elementary. With non-linear loads, the transient conditions must be taken into account to ensure that the specifications of the interface devices are not exceeded. Typical non-linear loads are lamps, whose cold filament surge currents are many times greater (5 to 15) than the quiescent hot filament, and dc motors, whose start and stall currents are often several times greater than run currents.

TABLE 2 – Approximate Values of ON Resistance

V_{DD} (Volts)	V_{OH} (Volts)	SOURCE $R_{ON(typ)}$	SOURCE $R_{ON(max)}$	V_{OL} (Volts)	SINK $R_{ON(typ)}$	SINK $R_{ON(max)}$
5.0	2.5	1.7 k	12.5 k	0.4	500	2 k
10	9.5	500	2.5 k	0.5	420	1 k
15	13.5	430	–	1.5	190	–

As shown in Figure 3, the transient response associated with these non-linear loads must be taken into consideration to adequately define the interface device and also to ensure that ratings are not exceeded.

Figure 3.1 illustrates the typical transient current, voltage and device dissipation of a lamp load being driven by an interface device that is not h_{FE} limited – it can supply all the current that the load demands. Under these conditions, the output voltage will quickly swing from its OFF state V_1 to ON state $V_{CE(sat)}$ in a time dictated by the transient response of the device. The peak current will be a function of the lamp's cold, low resistance filament and will decay exponentially as the lamp filament heats and resistance increases. This thermal response can last tens of milliseconds, depending on the rating of the lamp and filament size. The peak device dissipation, the product of the voltage and current, would be similar to that power waveform of Figure 3.1(c); this can be equated to the rectangular power pulse of 3.1(d) to simplify average power calculations. The peak dissipation resulting from these transient conditions must then be related to the device transient thermal response and Safe Operating Area (SOA) to ensure that average dissipation does not exceed the maximum ratings.

The case where the interface device is h_{FE} limited (where it cannot supply all of the peak current that the load demands) can result in even greater device dissipations. This is illustrated in the transient waveforms of Figure 3.2 where the peak current is less than in the previous example, but also where the device exits the saturation state during the switching transistions due to insufficient input drive current. The resulting power dissipation pulse can be excessive and destructive. For this reason, it is good engineering practice to design the interface device, be it a discrete or I.C., with adequate current gain under transient conditions. Obviously, the device must be able to sustain these peak currents. In cases where one has no control of the current gain and forced h_{FE} of the device, as in some I.C. high current logic devices, it is important to ensure that the device ratings are not exceeded.

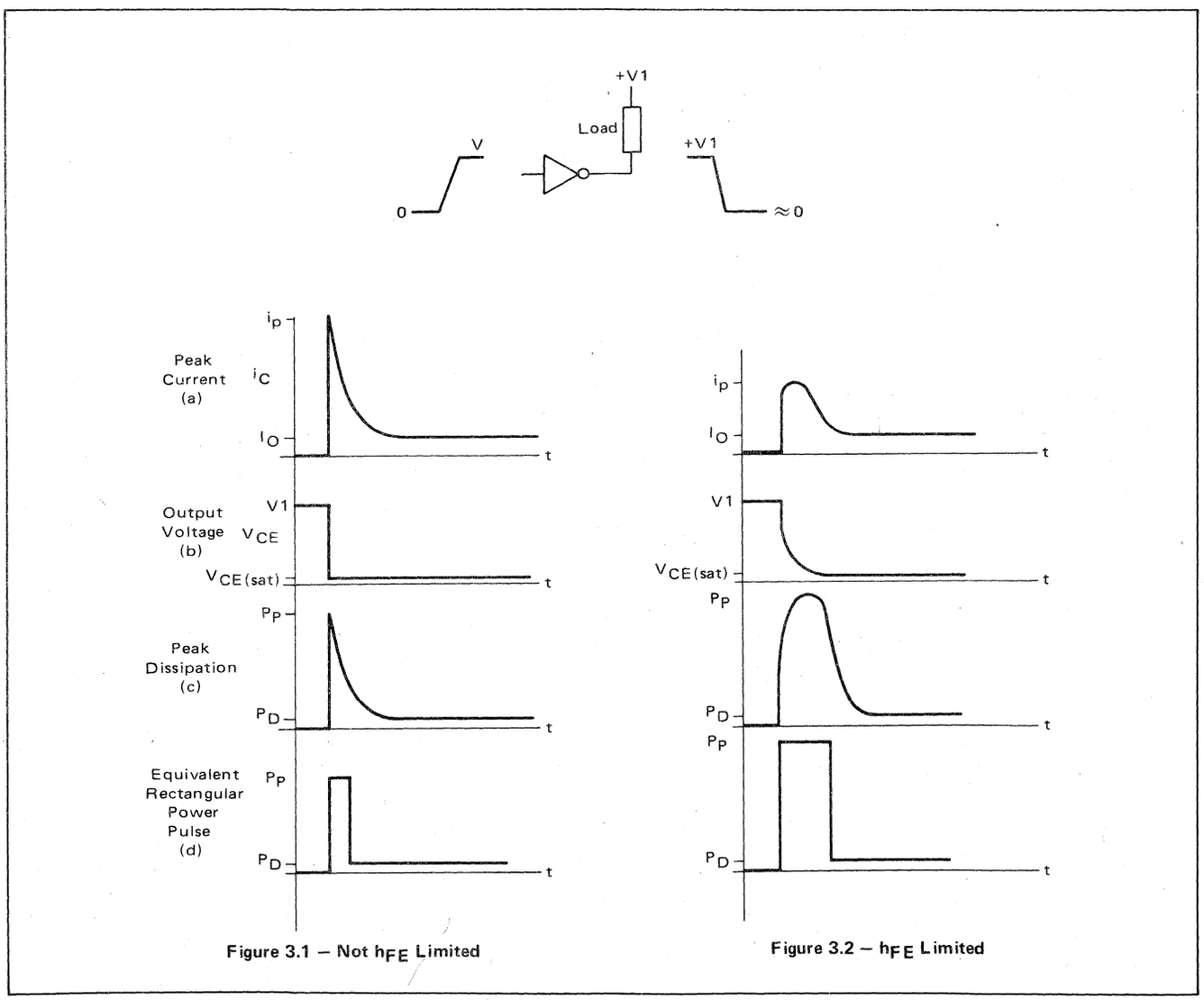


Figure 3.1 – Not h_{FE} Limited

Figure 3.2 – h_{FE} Limited

FIGURE 3 – TRANSIENT RESPONSE OF NON-LINEAR LOAD

These surge currents aren't limited only to lamp loads; they are also inherent in start-up and stall currents of dc motors. Also, as with any inductive load, be it motors or relays, it is mandatory that the reactive load line be within the devices safe operating area and that the device be protected with inductive voltage suppressors (i.e., clamp diodes, zeners, resistor-capacitor networks, etc.) so as not to exceed the breakdown voltage of the device.

INTERFACE DEVICE CHARACTERIZATION

To ensure that the interface device has adequate current gain under worst case design often requires extrapolation of the somewhat limited published information on the data sheet. As an example, a transistor might have $h_{FE(min)}$ and $h_{FE(typ)}$ specified at a current other than the current in question, with no typical h_{FE} vs current and temperature curves published. There also might be another $h_{FE(typ)}$ specified at a different current. By extrapolating the two typical h_{FE} points, the $h_{FE(typ)}/h_{FE(min)}$ ratio, the desired $h_{FE(min)}$ can then be roughly determined.

If the circuit is required to operate at some much lower temperature than the 25°C at which the device was characterized, than the above calculated $h_{FE(min)}$ must additionally be modified for consideration of low temperature operation.

Generally, h_{FE} falls off by an approximate 50 to 67% factor at -55°C. Once the minimum h_{FE} is determined, the circuit designer must decide on what forced h_{FE} and/or base overdrive factor to use to ensure that the transistor is saturated under worst case conditions (including worst case conditions of the driver logic device). The probability of all blocks in the circuit being worst-cased simultaneously must also be considered, particularly when this imposes undue current requirements on the logic driver. In that case, it might be necessary to make trade-offs on the worst case design with the current capability of the driver.

The example citied is for a bipolar transistor but the reasoning is applicable to any interface device, be it a thyristor with its maximum gate current requirements or an I.C. high current logic device with its limited drive current.

With these design guidelines as a basis, it becomes a relatively simple task to interface the industrial logic with the power devices. The following circuits illustrate these techniques where examples of various loads and power levels, both dc and ac, using bipolar transistors and thyristors as power devices are shown.

MHTL INTERFACE CIRCUITS

Perhaps the simplest circuit for interfacing between HTL logic and a non-linear load in the 1 to 5W range is shown in Figure 4. This figure illustrates the passive-pull up MHTL MC670 gate turning on a lamp driver transistor (activating the lamp) when the logic output goes low active state low).

The emitter of the PNP driver transistor is tied to the same +15V supply as the gate; when the logic output is high, the transistor is biased OFF and the lamp will be OFF. When the logic switches low, it must be able to sink the base current of the driver transistor and still be within it's maximum specifications (12mA). Thus, the limiting resistor R_1 is selected to furnish adequate base current to the driver transistor under worst case conditions: surge currents, minimum h_{FE}, and minimum operating temperature.

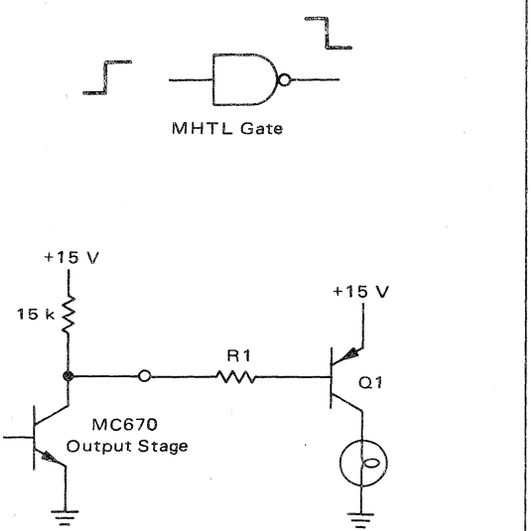
For the first example, Figure 4 condition (a), the 80mA lamp load with its high surge current and a forced gain of approximately 7 was selected resulting in a base current of approximately 11.5mA which is less than $I_{sink(max)}$ of 12mA. This results in a base current limiting resistor R_1 equal to

$$R_1 = \frac{V_{CC} - V_{CE(sat)} - V_{BE_1}}{I_B} = \frac{15 - .3 - .7}{11.5} \approx 1.2K$$

An inexpensive, small-signal, plastic PNP transistor (2N4403) was selected as the interface driver. The pertinent specifications are:

I_{Cmax} = 600mA continuous, (well within the quiescent lamp current of 80 mA).

$h_{FE_{min}}$ = 100 @ I_C = 50 mA
= 100 @ I_C = 150 mA.



CONDITION	LOAD	Q1	R1
(a)	Lamp CM330 14 V @ 80 mA	2N4403	1.2 k
(b)	Lamp 1816 13 V @ 350 mA	2N6296 Darlington	2.7 k

FIGURE 4 – MHTL LOGIC, PASSIVE PULL-UP, ACTIVE: LOW

The h_{FE} versus collector current curve can be presumed flat between the two specified points resulting in a minimum h_{FE} of 100 to 80mA.

Low temperature operation (-30°C, the maximum operating temperature of MHTL) may produce a lowering of h_{FE} to approximately 70% of that at 25°C, resulting in a minimum h_{FE} of about 70. This worst case h_{FE} results in a base overdrive factor of $\frac{h_{FE_{min}}}{h_{FE_{forced}}} = \frac{70}{7} = 10$ ensuring that the transistor is saturated for steady-state conditions.

However, the cold filament surge current may be greater than ten times steady state (approximately 800mA) and lasting for tens of milliseconds. Although this peak current exceeds the maximum continuous current of 600mA, it is within the published SOA pulse curve of one second at 1 ampere. This one second pulse is predicated on the lamp's thermal response being less than that period.

Secondly, with a base current of 11.5mA and a minimum h_{FE} of 70, a collector current of 800mA (11.5 x 70) can result before the transistor comes out of saturation. Thus, under worst case conditions, where the lamp surge current is 10 times steady state, the transistor will be saturated and the dissipation will be minimal. For this particular circuit, a surge current of 570mA lasting for 15 milliseconds was measured with the collector voltage driven sharply into saturation (Figures 3.1 (a) and (b)).

For high temperature operation, particularly when the circuit is de-activated (active logic high, Q_1 OFF), a resistive shunt path for I_{CBO} leakage current is provided through resistor R_1 and the 15 k pull-up resistor. For larger lamp currents to still be within the logic drivers 12 mA sink capability, the 350 mA lamp of Figure 4 condition (b), requires a higher h_{FE} transistor such as a Darlington with a forced h_{FE} of approximately 70.

The 2N6296, a PNP metal packaged TO-66 Darlington with built in base-emitter resistors and maximum continuous collector current of 4 amps, was selected. After extrapolating the published $h_{FE(typ)}$ versus collector current and temperature curves and the minimum specified h_{FE} at 2A, an $h_{FE(min)}$ at 350mA and -30°C was approximated to be 250.

If the base current were approximately 5mA, a forced h_{FE} for steady state conditions would be $\frac{350}{5} = 70$ with a resulting base overdrive factor of $\frac{250}{70} \cong 3.5$. The limiting resistor R_1 would be

$$R_1 = \frac{V_{CC} - V_{OL} - V_{BE_{Darlington}}}{I_B}$$

$$= \frac{15 - .2 - 1.3}{5mA} \cong 2.7\ k.$$

This results in a saturated circuit under steady state conditions, but with minimum h_{FE}, low temperature, surge current operation, the transistor could pull out of saturation with an associated increase in dissipation. However, even under these worst case conditions, the transistor is operating within its SOA.

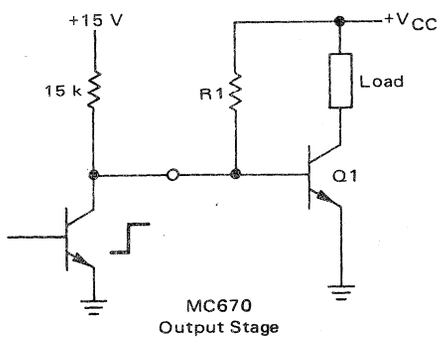
The case where the passive pull-up gate activates the load when the logic output goes high is shown in Figure 5 for such non-linear loads as the previously mentioned lamps and a small instrument type dc motor.

The circuit is de-activated when the logic output is low (saturated) clamping the interface transistor base-emitter OFF. Although the published $V_{OL(max)}$ ($V_{CE(sat)}$) for the MC670 is 1.5V to encompass the complete MHTL family of gates, in reality, the maximum saturation voltage would be approximately 0.4V with typical values being in the 0.1 to 0.2V range at 5 to 10mA sink currents. This low value of V_{OL} thus ensures proper clamping.

When the logic output goes high (the gate output transistor cut-off), the internal 15 k collector resistor then supplies the base current and would be approximately 1mA ($\cong \frac{15V}{15\ k}$). For larger base current requirements, the pull-up resistor R_1 in parallel with the 15k collector resistor furnishes the current. This parallel resistor combination must be within the sink current capability of the gate.

The table of Figure 5 describes the transistor types and pull-up resistors for the various loads. As in the previous examples, the transistors and resistors were chosen to satisfy the surge current requirements of the load.

For Figure 5 condition (a), using the MPS-A13 Darlington transistor, no pull-up resistor is required since this device has adequate h_{FE} to be saturated by the sourcing of the MC670.



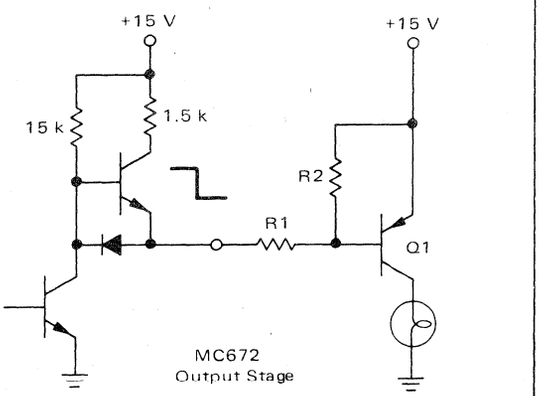
CONDITION	LOAD	V_{CC}	Q1	R1
(a)	Lamp 14 V @ 80 mA	15 V	2N4401	8.2 k
			MPSA13 Darlington	∞
(b)	Lamp 13 V @ 350 mA	15 V	2N6294 Darlington	2.7 k
(c)	D.C. Motor 24 V @ 65 mA	24 V	2N4401	8.2 k

FIGURE 5 – MHTL, PASSIVE PULL-UP, ACTIVE: HIGH

Additionally, for these configurations, the supply voltage need not be the +15V but can be of any magnitude as required by the load; the only requisites of the interface transistor, in addition to having adequate h_{FE}, is that the circuit operates within the SOA curve.

When using active pull-up MHTL gates, the sinking current criteria of the gate is almost identical to the passive pull-up case. The basic difference between the two devices is that $V_{OL(max)}$ for the active pull-up gate (MC672) is 1.5V to consider the internal diode drop ($V_{OL} = V_{CE(sat)} + V_D$) whereas the MC670 $V_{CE(sat)}$ is approximately 0.2V.

Figure 6 illustrates an active pull-up gate activating the load when its logic output goes low. The base current limiting resistor R_1 is chosen to be within sink capability of the logic device and still provide adequate drive to the interface PNP transistor under worst case conditions. When the logic swings high, transistor Q_1 is at cut-off (the load de-energized). Resistor R_2 is required for leakage current by-pass considerations. When using the 2N6296 Darlington transistor as the interface device [Figure 6 condition (b)], R_2 is not required as this transistor has built in base-emitter shunt resistors for I_{CBO} effects.



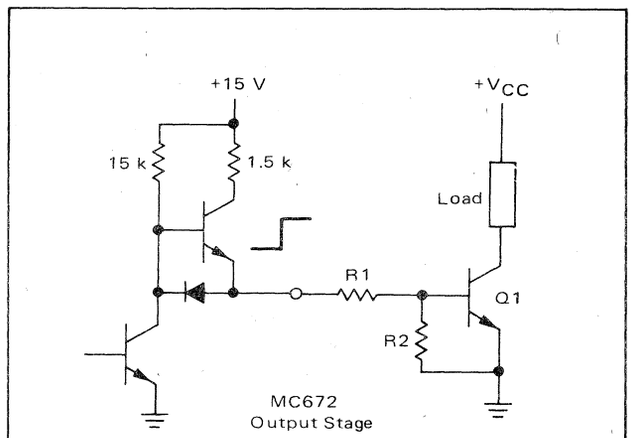
CONDITION	LOAD	Q1	R1	R2
(a)	Lamp 14 V @ 80 mA	2N4403	2.2 k	10 k
(b)	Lamp 13 V @ 350 mA	2N6296 Darlington	3.3 k	∞

FIGURE 6 – MHTL LOGIC, ACTIVE PULL-UP, ACTIVATION: LOW

An example of how the load is activated when the MC672 logic goes high is shown in Figure 7. Again, the base limiting resistor R_1 is designed to furnish adequate drive to the NPN transistor. The limiting value of this resistor would be zero ohms (Figure 7 condition (a)) where the base current (source current of the MC672) would be approximately the short-circuit current of the logic device. Under this condition, the high logic output would be clamped to the base-emitter voltage of the interface transistor (0.7V) and could not be used to drive some other circuit. By making R_1 finite, the high logic level would now be dictated by its equivalent emitter follower driver and its load (R_1+Q_1) and may now be predictably high enough to drive other logic circuits.

The load (and Q_1) is de-energized when the logic output goes low. Under these conditions the active pull-up transistor is at cut-off, the logic driver is saturated and base drive to the interface transistor is removed, also cutting it off. Resistor R_2 is necessary to reduce leakage current of Q_1 and should be designed for maximum operating temperature I_{CBO} considerations.

The case of an active pull-up MHTL device whose high output level activates an NPN Darlington transistor for high current gain is illustrated in Figure 8. In this example, a base current of 6mA is required to ensure adequate drive. The MHTL gate cannot completely source



CONDITION	LOAD	V_{CC}	Q1	R1	R2
(a)	Lamp 14 V @ 80 mA	+15 V	2N4401	2.2 k	4.7 k
				0	4.7 k
(b)	D.C. Motor 24 V @ 65 mA	+24 V	2N4401	2.2 k	4.7 k

FIGURE 7 – MHTL, ACTIVE PULL-UP, ACTIVATION: HIGH

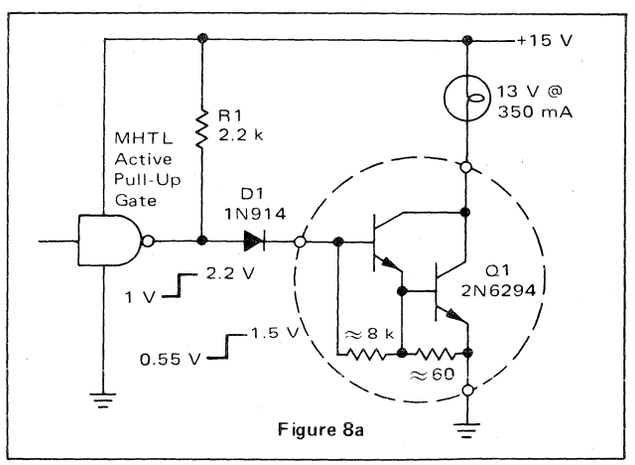


Figure 8a

this current and still ensure a V_{OH} compatible with the Darlington. However, by adding the pull-up resistor R_1 to source the major part of the current, the circuit is made reliable. Diode D_1 is added to ensure that the maximum low level logic output ($V_{OL(max)}$ = 1.5V) will not turn on the two cascaded emitter-base junctions of the Darlington.

The logic high level output will be clamped to approximately 2.2V, the two emitter-base voltage drops plus the diode drop, making this level incompatible for driving other logic circuits.

A technique for overcoming this condition is shown in Figure 8(b). Diode D_1 isolates the high logic output from the interface circuit allowing the output to swing to V_{CC} less one emitter-base drop (15-5 = 14.5V). Diode D_3 is required to compensate for diode D_1 drop (when the logic goes low) and thus ensure that the Darlington is cut-off.

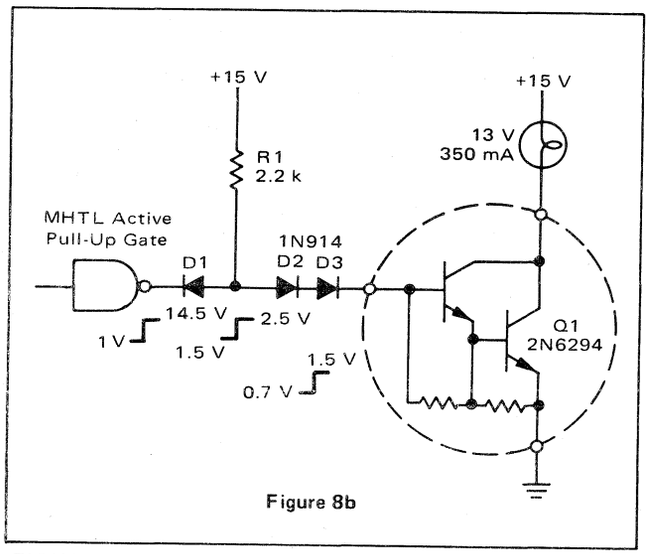


FIGURE 8 – HIGH LEVEL, MHTL ACTIVE PULL-UP OUTPUT INTERFACING WITH NPN DARLINGTON

When the load is powered by a voltage greater than the MHTL supply of 15V and when the MHTL low level output is required to activate this load, then the simple circuits of Figures 4 and 6 will not suffice. This is due to the logic V_{OH} being less than the base voltage of the PNP transistor and therefore possibly turning that transistor ON when it should be OFF.

By using a level translator transistor (Q_1 of Figure 9(a)) that is referenced to the MHTL supply, this shortcoming can be eliminated. When the logic level goes low, Q_1 is turned ON, which in turn energizes Q_2 and the load.

The base-emitter resistor R_2 is required for leakage current considerations of Q_1 when driven with an active pull-up logic device, but it is not needed for the passive pull-up case.

In some applications, where other loads are connected to MHTL output pulling it down (Figure 9(b)), a coupling zener diode D_1 is required to prevent the loaded V_{OH} from turning Q_1 ON. With the component values shown, the logic output can drop to approximately 7V before the load is erroneously energized.

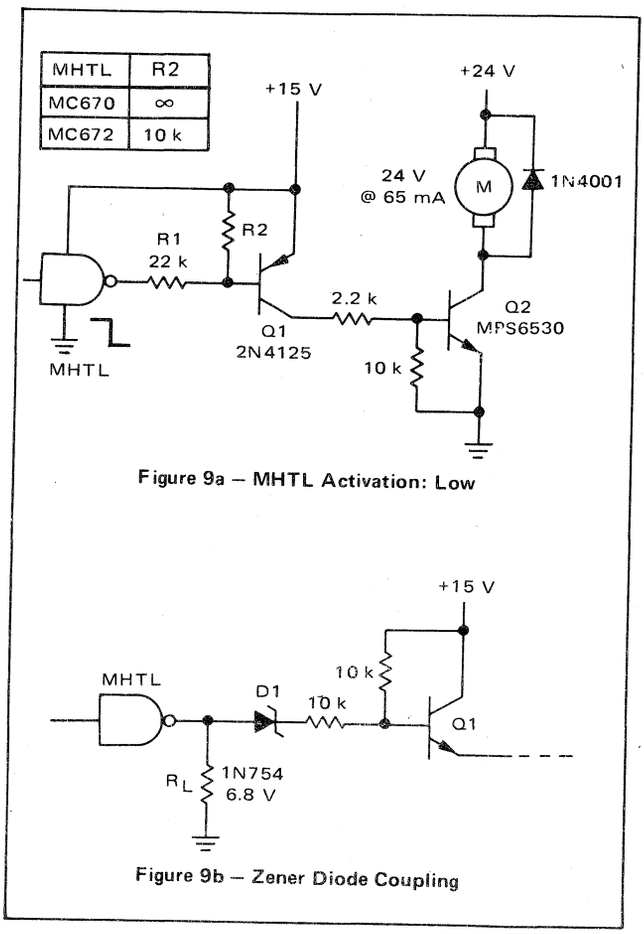


FIGURE 9 – MHTL INTERFACING WITH LOAD POWERED BY GREATER THAN +15 V SUPPLY

McMOS INTERFACE CIRCUITS

The second industrial logic family of particular interest is CMOS. As previously described, these logic devices can sink and source currents from fractions of milliamperes to approximately 10mA, depending on how high (or low) the acceptable output voltage may be. In many cases, where the load power requirements are relatively low, the CMOS gate can be directly interfaced to the load driver, assuming that ample power gain is available.

Figures 10(a) and (b) illustrate a typical CMOS gate (1/4 of a quad 2-input NAND Gate/Inverter MC14011) directly interfacing with small signal plastic Darlington transistors driving an 80 mA lamp load. The first example describes a low level output driving a PNP Darlington MPS-A65; in the second case, the high output drives a complementary MPS-A13. With the component values shown, the respective sink and source currents are approximately 350 μA resulting in V_{OL} and V_{OH} (due to R_{ON}) being approximately 0.04 and 14.8 V, respectively.

In addition to driving bipolar transistors, the CMOS gates can directly drive sensitive gate SCRs (Figure 10(c)).

This circuit shows a small-signal, plastic TO-92 case 2N5060, with a maximum gate trigger current I_{GT} at low temperatures (-65° C) of 350μA being directly triggered by the CMOS gate high level output. The 39 k current limiting resistor will supply the approximate 350μA (more than adequate for -55° C McMOS operation) and still maintain V_{OH} (approximately 14.8V) at acceptable levels for driving other CMOS logic.

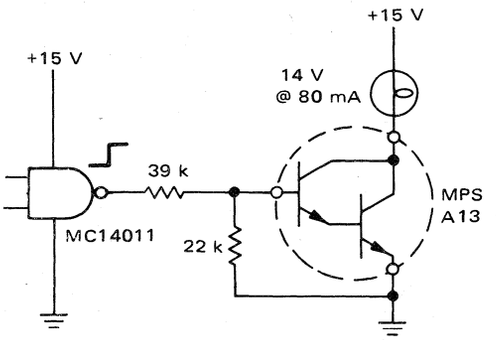


Figure 10b – CMOS High Level Activation, Bipolar Interface

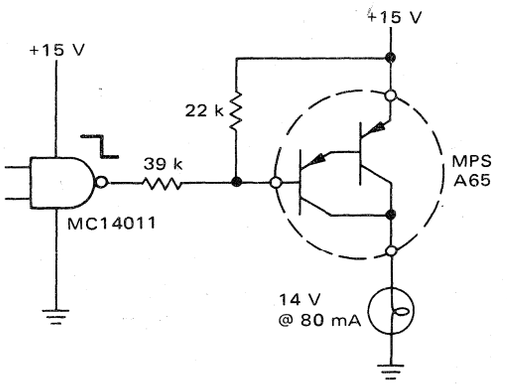


Figure 10a – CMOS Low Level Activation, Bipolar Interface

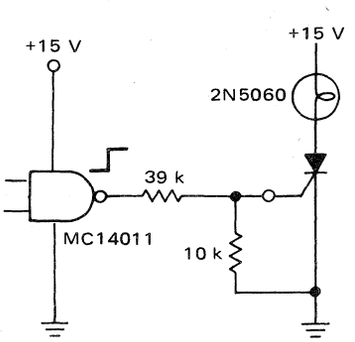
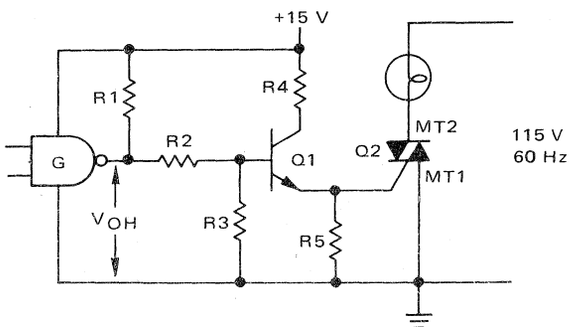


Figure 10c – CMOS High Level Interfacing With Sensitive Gate SCR

FIGURE 10 – INTERFACE TECHNIQUES BETWEEN CMOS AND LOW POWER LOADS



THYRISTOR CONTROLLED AC LOADS

The amount of power that these industrial logic families can control is virtually unlimited; the major criteria is that the interface devices have suitable power gain. Previous circuits have illustrated simple low power dc systems. The following examples, Figures 11 through 14, show how to interface with higher power ac loads using thyristors as the ac control element.

Figure 11 describes the interface configuration of high level activation of both MHTL and McMOS gates with triac controlled ac loads. The active logic one level output turns-on the effective common-emitter transistor Q_1, whose emitter current, as determined by its collector resistor R_4, positive gate triggers the triac. This gate current is designed for maximum I_{GT} at -40°C, (gate

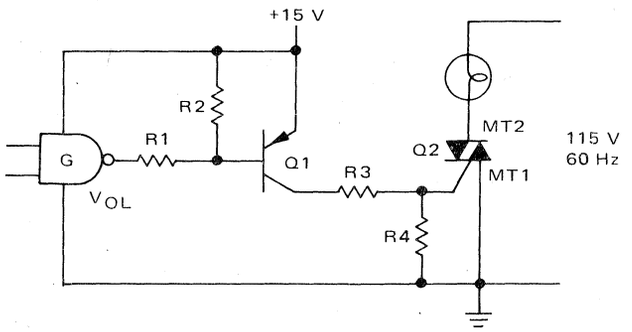
CONDITION	LOGIC DEVICE G	LOAD	Q1	Q2	R1	R2	R3	R4	R5	V_{OH}typ
(a)	MHTL MC672	300 W	2N4401	MAC10-4	∞	2.2 k	10 k	150 2 W	∞	9 V
(b)	MHTL MC670	300 W	2N4401	MAC10-4	5.6 k	0	∞	150 2 W	∞	1.7 V
(c)	McMOS MC14011	25 W	2N4401	MAC92A-4	∞	12 k	10 k	560 1 W	1 k	14.6 V
(d)	McMOS MC14011	300 W	2N4401	2N6346	∞	2.2 k	10 k	110 4 W	∞	12.8 V

FIGURE 11 – INTERFACING BETWEEN LOGIC AND AC LOADS, ACTIVATION: HIGH

sensitivity falls off with decreasing temperature) which for the three triacs used, MAC10-4, MAC92A-4 and 2N6345, are approximately 90, 25 and 125mA, respectively.

The MAC92A-4 is a sensitive gate triac and typically requires a 1 k resistor between the gate and Main Terminal 1 to desensitize the device to noise transients. The other two triacs have internal resistors built in and require no desensitizing.

The NPN transistor Q_1 must have adequate current gain for worst case conditions to interface between the logic sourcing capability and the triac triggering requirement. Its input network is dictated by which logic device



CONDITION	LOGIC DEVICE G	LOAD	Q1	Q2	R1	R2	R3	R4	V_{OL} typ
(a)	MHTL MC672	300 W	MPS3638A	MAC10-4	2.2 k	10 k	150 2 W	∞	1.1 V
(b)	MHTL MC670	300 W	MPS3638A	MAC10-4	2.2 k	∞	150 2 W	∞	0.25 V
(c)	McMOS MC14011	25 W	MPS3638A	MAC92A-4	12 k	10 k	560 1 W	1 k	0.15 V
(d)	McMOS MC14011	300 W	2N4403	2N6346	3.9 k	10 k	110 Ω 4 W	∞	0.50 V

FIGURE 12 – INTERFACING BETWEEN LOGIC AND AC LOADS, ACTIVATION: LOW

is used, the MC670 requires a pull-up resistor R_1 for increased current sourcing and is directly coupled to the Q_1 base, whereas the MC672 and MC14011 can source adequate current through a limiting resistor R_2. The sourcing current in the 300W circuits is approximately 3mA, whereas for the 25W circuit, (Figure 1, condition (c)) approximately 1mA. For the CMOS gates, the effect of R_{ON} is apparent in the value of V_{OH} for the two different sourcing current cases (1 and 3mA) being 14.6 and 12.8V respectively.

When an active low level logic is required to activate the load, the interface circuits of Figure 12 will suffice. These circuits are basically the complement of Figure 11 in that the logic zero sinks the base current of the PNP transistor Q_1 and drives it into saturation. The collector current of Q_1, determined by R_3, supplies the positive gate current to the triac Q_2 turning it and the load ON.

The gate sink currents are approximately the same as those in Figure 11 (1 and 3mA), with V_{OL}, for the CMOS gates, being approximately 0.15 and 0.50V respectively, illustrating that $R_{ON(sink)}$ is less than $R_{ON(source)}$.

Triacs can be triggered with both positive and negative gate currents with four combinations of gate current and Main Terminal 2 (MT2) voltages possible. The most sensitive mode, or quadrant, is when the gate and MT2 are positive with respect to MT1 (quadrant 1); the least sensitive is Quadrant 4 when the gate is positive and MT2 is negative.

When gate sensitivity for logic current drive capability is a criteria for switching an a.c. load, it is recommended to use negative gate trigger current with its associated nominal sensitivity, (quadrants 2 and 3). The circuits of Figures 13(a) and (b) illustrate both high and

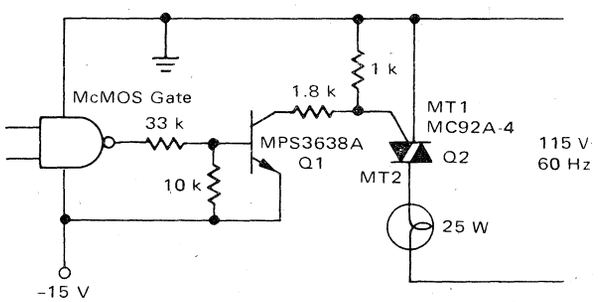


Figure 13a – Active: High

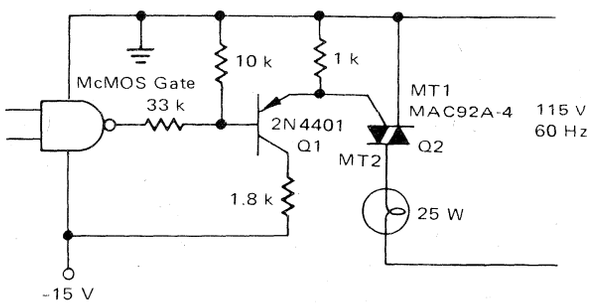


Figure 13b – Active: Low

FIGURE 13 – McMOS INTERFACING WITH SENSITIVE GATE TRIAC USING A NEGATIVE SUPPLY

low CMOS logic activating the 25W load. To achieve the negative gate current (current flowing out of the gate) requires that the logic and interface transistor high supply line be grounded and the low line attached to the negative supply. The maximum negative gate current at -40° C required to fire the triac is specified as 8mA whereas the quadrant 4 current is 25mA (Figures 11 condition (c) and 12 condition (c)). Thus, both the drive transistor Q_1 and the CMOS gate output current can be scaled down by that approximate 3:1 ratio.

In the previous examples, the triac gate current was supplied by a transistor switch referenced to the logic gate supply, which as in the case of Figure 11 condition (d) using the 2N6346, required a worst case gate current of approximately 125mA.

This relatively large power supply drain can be excessive in some applications. The circuit of Figure 14, using capacitor storage techniques, overcomes this problem and operates as follows. Storage capacitor C_2 completely charges to V_{CC} (+15V) in $5R_3\ C_2$ time constants, at which some short time later transistor Q_1 is fired by the positive-going differentiated pulse derived from the input square wave. Capacitor C_2 dumps its charge through the limiting resistor R_4 and the ON transistor Q_1 causing triac Q_2 to be fired and energizing the a.c. load. To have maximum power delivered to load, the triac should be fired early in its conduction angle. As an example, if the triac is fired at a conduction angle of 18°, greater than 99% of the power is delivered, at 30°, approximately 97%. When the input square wave trigger is 1kHz, the greatest change in conduction angle $\Delta\theta$ on a cycle to cycle basis for a 60Hz load is approximately:

$$\Delta\theta_{max} = \frac{360^\circ}{(1KHz/60Hz)} \text{ or } 21.6^\circ,$$

and the minimum output power is approximately 98% of the maximum available. The period of the trigger ($\frac{1}{1\ kHz}$ = 1 millisecond) is greater than the five time constants of the storage network [5(1.5 k) (0.1μf) = 750μsec] to

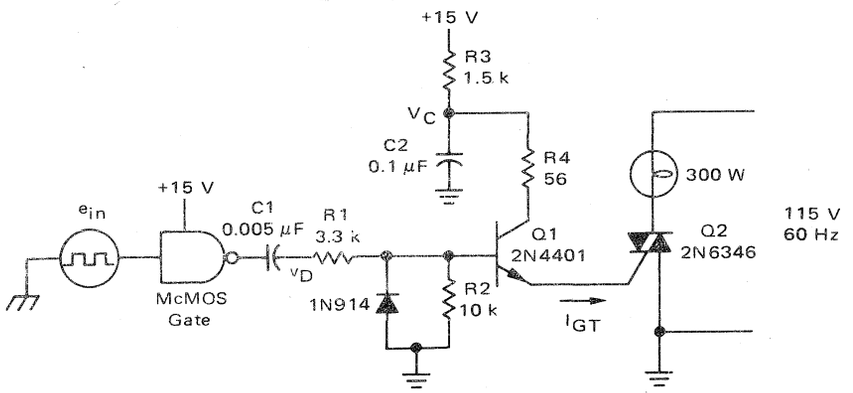


Figure 14a

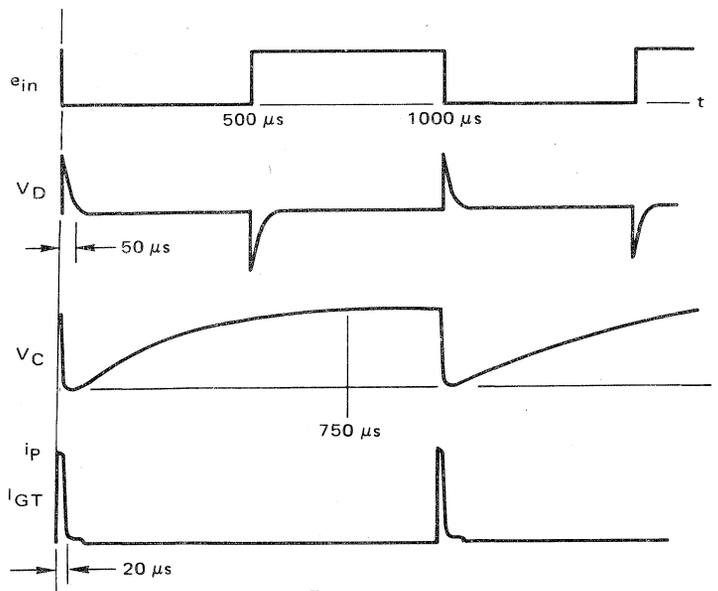


Figure 14b

FIGURE 14 – McMOS DRIVING TRIAC USING CAPACITOR STORAGE TECHNIQUES

ensure that the capacitor is completely charged. To ensure rapid triac turn-on, and thus minimize the effects of $\frac{di}{dt}$, it is recommended to fire the device with a fast rise-time, high current pulse (within its ratings). The minimum specified gate pulse width for the 2N6346 triac is 2μsec; therefore, transistor Q_1 should be ON for greater than this minimum time, as determined by the differentiating time constant (R_1 + R_{ON} CMOS) C_1 to allow the storage capacitor to discharge through R_4, Q_1 and the input of Q_2. Current limiting resistor R_4 sets the peak current and with C_2 determines the pulse width. The circuit waveforms of Figure 14(b) show the gate trigger current waveform to be approximately 200mA peak and 20μsec wide.

The average +15V power supply drain was measured as 4mA relative to the 125mA drain of the d.c. coupled example of Figure 11, condition (d).

HIGH CURRENT LOGIC DRIVERS

There are several high current industrial logic I.C. drivers that readily interface with compatible loads. In the MHTL family, the MC679 Dual Lamp Driver can sink 150 mA, as shown in Table 3. The McMOS family is represented by the MC14009, MC14049 and MC14010, MC14050 which are Hex Inverter/Buffers and Non Inverting Hex/Buffers, respectively. The MC14009/10 and MC14049/50 can typically sink 35 and 40mA respectively. Also illustrated in this table are other families of high current logic drivers, MTTL and Linear, capable of interfacing directly with higher power loads.

Examples of low power industrial logic interfacing with these higher power drivers are shown in Figure 15. Figure 15(a) describes a typical McMOS gate, MC14011AL driving the MC679 Lamp Driver. To energize the load, the McMOS output goes high driving the MHTL output low. To turn the load OFF, the MC14011AL must be able to sink the MC679 forward current I_F of 1.2mA maximum and still have a $V_{OL(max)}$ less than the MHTL threshold of 6.5V minimum. With a +15V supply, the MC14011AL has a specified $V_{OL(typ)}$ of approximately 0.4V at an I_{OL} of 1.2mA and a temperature of 85°C (at a constant I_{OL}, V_{OL} increases with increasing temperature). Although worst case I_{OL} is not specified, from the previous calculations of $R_{ON(max)}$ of Table 2, R_{ON} for the sink condition can be assumed to be no greater than 1 k. The simple voltage divider calculation of R_{ON} with the MHTL input pull-up resistor of 15 k would result in a $V_{OL(max)}$ of approximately 1V and well within the 6.5V threshold.

The second circuit, Figure 15(b), illustrates the interfacing between McMOS and MTTL MC7406 30V, 40mA, Hex Inverter Buffer/Driver. Since the MTTL I.C. is a 5V device, the McMOS also operates from this supply. The forward current I_F of the MC7406 is 1.6mA and is well within the worst case of the McMOS buffer sink capability of 2.1mA at a supply of 5V, V_{OL} of 0.4V (max TTL V_{OL}) and a temperature of 125°C.

The high current logic drivers are well-suited for driving Light Emitting Diodes (LED). An example of a visible red LED, made of gallium arsenide phosphide, being driven by a McMOS buffer is shown in Figure 15(c). The sinking current of this gate is within the typical LED current of 10mA where the limiting resistor R is dictated by this current, the supply V_1, the LED drop of 1.6V typical, and the low level output voltage V_{OL} of the driver.

Higher current loads can be directly interfaced with McMOS buffers when there is adequate power gain in the interface device. An example of such a circuit driving a 3A load, using the 2N6055 8A Darlington transistor, is shown in Figure 15(d). Worst case h_{FE} at -55°C and collector

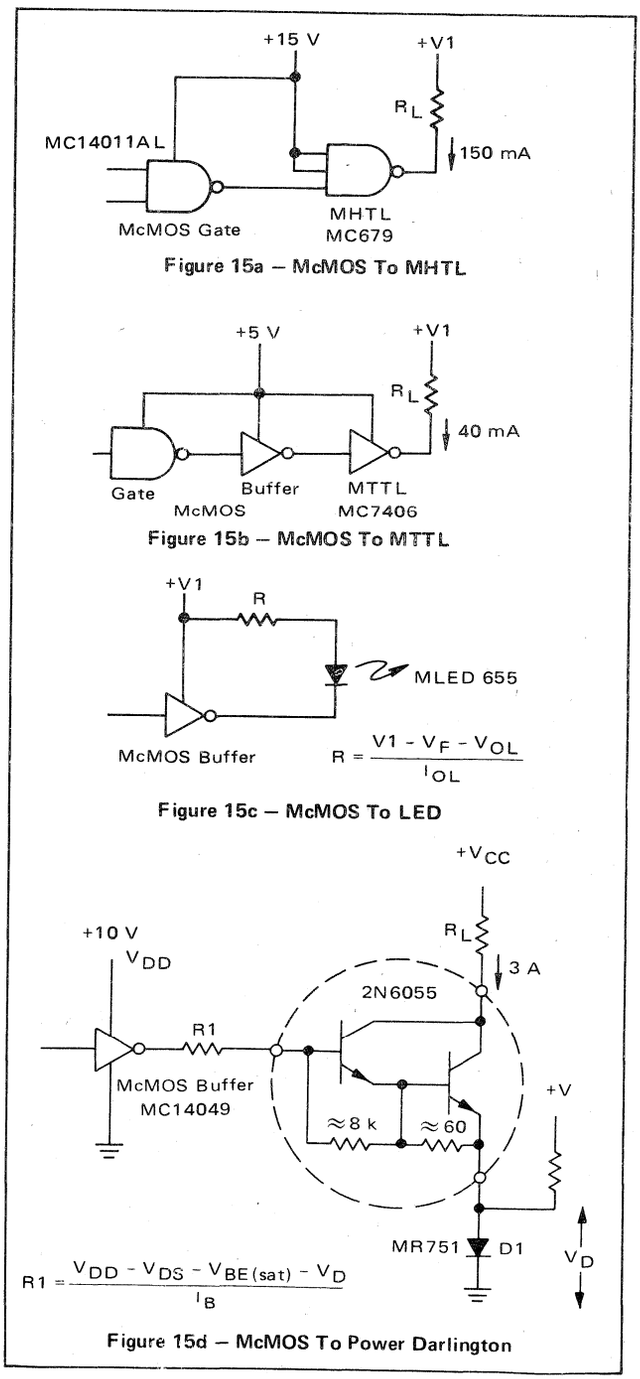


Figure 15a – McMOS To MHTL

Figure 15b – McMOS To MTTL

Figure 15c – McMOS To LED

Figure 15d – McMOS To Power Darlington

FIGURE 15 – TYPICAL HIGH CURRENT LOGIC DRIVER CIRCUITS

TABLE 3 – High Current Logic Drivers

Product Family	Device Number	Description	V_{CC} or V_{DD}	$V_{I(max)}$	I_O	Remarks
MHTL	MC679	Dual Lamp Drivers	15 V	30 V	150 mA Max	Open Collector
McMOS	MC14009 MC14010	Hex Inverter/Buffer Non-Inverting Hex Buffer	V_{DD} = 3 to 18 V	$V_{CC} \leqslant V_{DD}$	$I_{OL(typ)}$ = 35 mA @ V_{CC} = 15 V, V_{OL} = 1.5 V	Requires Two Supplies $V_{CC} \leqslant V_{DD}$
	MC14049 MC14050	Hex Inverter/Buffer Non-Inverting Hex Buffer	3 to 18 V		$I_{OL(typ)}$ = 40 mA @ V_{CC} = 15 V, V_{OL} = 1.5 V	One Supply $I_{O(max)}$ = 45 mA
MTTL	MC7406	Hex Inverter Buffer/Driver	5 V	30 V	$I_{sink(max)}$ = 40mA	Open Collector
Linear	MC55325	Dual Memory Driver	5 V	24 V	I_O = 600 mA @ V1 = 15 V	Contains 2 Sink Switch Pairs and 2 Source Pairs
	MC75450	Dual Peripheral	5 V	30 V	300 mA	TO-116 14 Pin Case
	MC75451	Positive "AND" Driver				8 Pin Plastic Case
	MC75452	"NAND" Driver				Open Collector
	MC75453	"OR" Driver				
	MC75454	"NOR" Driver				
	MC75491	Multiple LED Driver Quad Driver	10 V Max	–	I_{source} or I_{sink} = 50 mA	MOS to LED Darlington Drivers
	MC75492	Hex Driver			I_{sink} = 250 mA	

current of 3A was approximated to be 500. Using a base overdrive factor of 3 to 1 results in a base current of approximately 18mA, a current well within the sourcing capability of McMOS Buffer MC14049. For high temperature operation, it is recommended that diode D_1 be placed in the emitter of the Darlington. This ensures reverse biasing of the Darlington in the OFF state and thus prevents thermal runaway.

OPTOELECTRONIC COUPLERS

When a LED is integrally packaged with a photodetector, an optoelectronic coupler is achieved. Typically, the LED is of gallium arsenide, infrared light emitting type, whereas the detector can be a single photo transistor or Darlington.

These optoelectronic couplers are designed for applications requiring electrical isolation and have input/output isolation voltages as great as 2500V with isolation resistances being typically in the 10^{11} ohm range. Due to the high isolation properties of these couplers and an inherent band width capability of from dc to (in some cases) 300kHz, they can be readily used where it is required to isolate higher voltage and power loads from the low level logic. The coupling from logic to load is simplified as the device can replace a dc coupled system with its associated general requirement for level translation, and a pulse transformer or coupling capacitor with their limited bandwidth. Isolation is complete between the logic and the load in that the power supplies and their circuit grounds can be completely independent from each other.

Motorola manufactures a complete series of optoelectronic couplers and some of these devices are listed with their characteristics in Table 4. Examples of circuits

TABLE 4 – Motorola Optoelectronic Couplers

Optoelectronic Coupler	Photo Detector Type	Isolation Voltage Min	D.C. Current Transfer Ratio Min	Detector Working Voltage Min	Bandwidth Typ
4N25	Photo Transistor	2500 V	20%	BV_{CEO} = 30 V	300 kHz
4N26		1500 V			
4N27			10%		
4N28		500 V			
4N29	Photo Darlington Transistor	2500 V	100%	BV_{CEO} = 30 V	30 kHz
4N30		1500 V	100%		
4N31		1500 V	50%		
4N32		2500 V	500%		
4N33		1500 V	500%		

using these devices for interfacing between CMOS logic and D.C. and A.C. loads are shown in Figures 16 through 19.

The first example, Figure 16, illustrates the 4N25 photon-coupler interfacing between the McMOS buffer and a 350mA d.c. powered lamp load. The lamp is normally de-energized when the 4N25 is energized. A high level on the input of the McMOS inverter energizes the opto-coupler, clamping the base-emitter junction of the NPN transistor Q_1 OFF. The NPN transistor removes drive to the following PNP transistor Q_2, thus de-energizing the load. Energizing the load requires removing the clamp and de-energizing the opto-coupler with a logic zero applied to its input. With the component values shown, approximately 10mA of input opto-coupler current can control a completely isolated 350mA load.

When greater sensitivity and current gain are required, the 4N29-33 series of optoelectronic couplers can be used. These devices, utilizing photo Darlington transistors as the detector, have minimum dc current transfer ratios I_C/I_F (the Darlington collector current to LED forward current) of as great as 100%.

A circuit for isolated, half wave a.c. control using the 4N26 opto-coupler, is shown in Figure 17. The detector is used as a static series switch in the gate circuit of the 2N5064 SCR. When the logic input goes high, the opto-coupler is energized allowing 2N5064 SCR principal current to flow. This current turns-on the power SCR and the load for that positive half cycle of the a.c. line voltage. Conversely, when the logic goes low, the coupler is de-energized, removing the 2N5064 gate current and the load current will cease at the next zero excursion of the a.c. source. Thus, with only approximately 5 mA of isolated dc control current, a half-wave load using the MCR106-4 of up to 4A can be controlled.

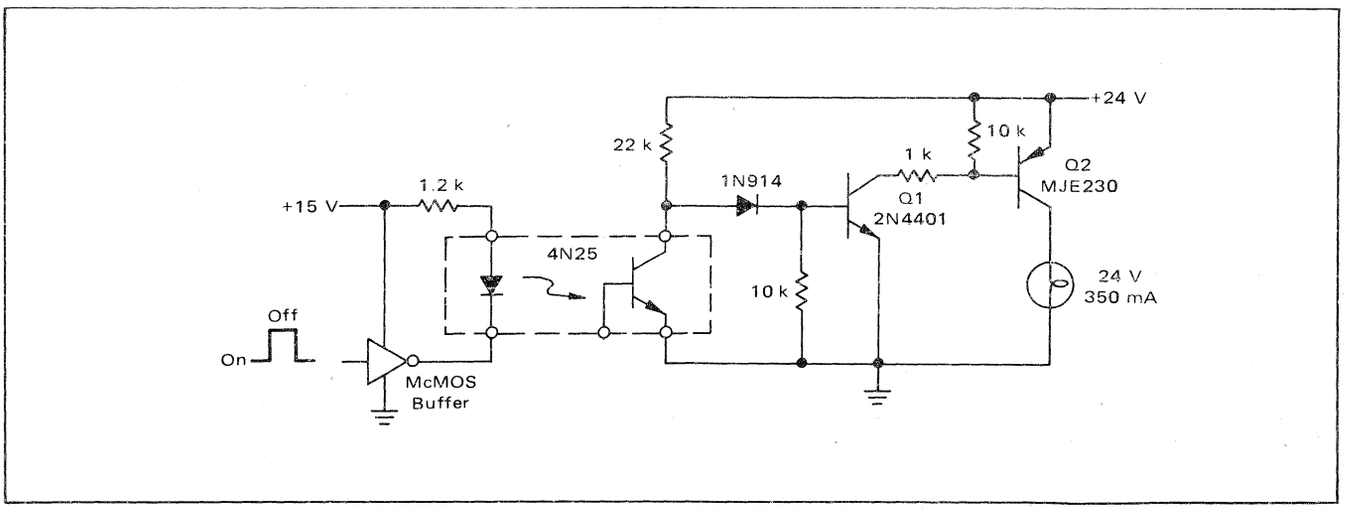


FIGURE 16 – DC CONTROL USING THE OPTOELECTRONIC COUPLER 4N25

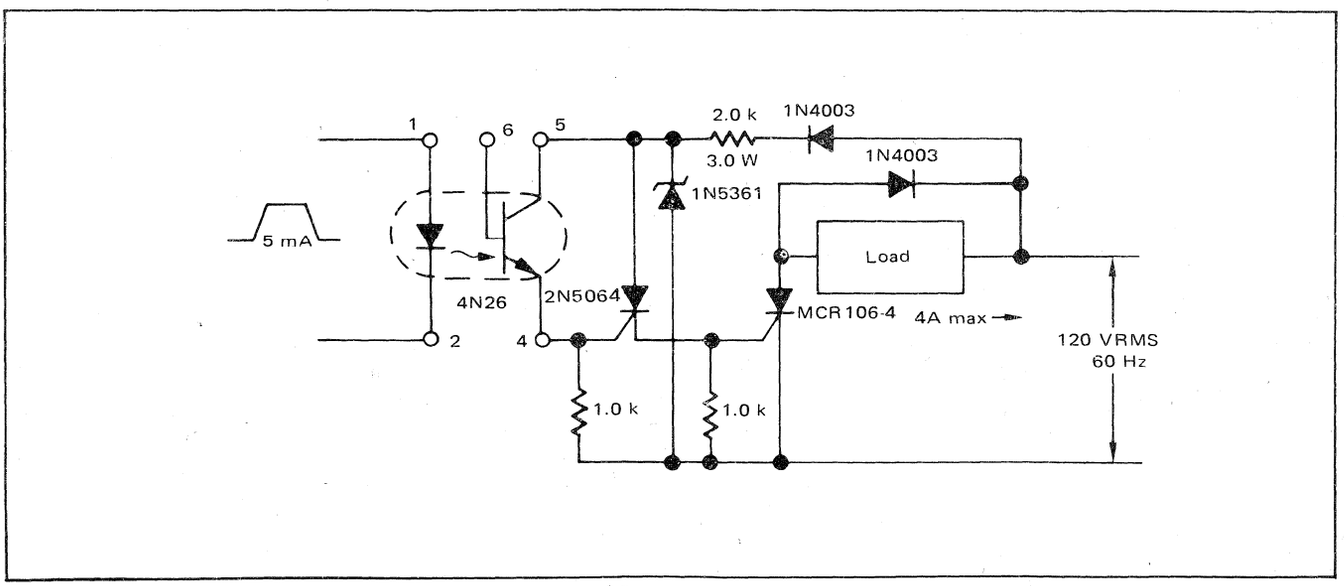


FIGURE 17 – HALF WAVE AC CONTROL USING THE 4N26

Isolated full-wave control of an ac load using the 4N26 and the 2N6071B sensitive gate triac can be readily implemented, as shown in Figure 18. For full-wave operation of the 2N5064, a bridge rectifier is required to convert the bidirectional ac line voltage into a unidirectional (full-wave rectified) voltage. The SCR is placed across the bridge dc output; when it conducts, a path for the triac gate trigger current is completed through the bridge and the SCR. Thus, a high level logic input energizes the optoelectronic coupler which triggers the SCR, and provides gate current for the triac.

The load will turn-on immediately upon application of the logic signal (less propagation delays), which, when it occurs other than at zero crossings of the ac line, can produce excessive EMI.

A circuit for overcoming this characteristic is illustrated in Figure 19. It consists of triac Q_1 with its trigger circuit R_1, C_1, S_1 and a clamp circuit consisting of the 4N26, 2N5064 SCR and bridge rectifier. To energize the load, the logic input goes low, the opto coupler is de-energized and the clamp is removed from across the trigger capacitor C_1 allowing it to charge through timing resistor R_1. When the voltage across the capacitor reaches the triggering voltage of S_1 (approximately 8V), the silicon bidirectional switch MBS4992 fires allowing the capacitor to dump the charge into the gate of the triac turning it and the load ON. Capacitor C_1 is chosen large enough to supply adequate trigger current to the triac and with its timing resistor R_1, the time constant is chosen small enough to fire the triac early in its conduction angle (near zero crossing) thus minimizing EMI and maximizing the power delivered to the load.

To de-energize the load, the logic high input energizes the opto-coupler which, with the SCR and bridge rectifier, clamps the trigger capacitor, thus inhibiting the triac from firing. The 1N5361 zeners are used, in the last three examples, to limit the voltage applied to the coupler transistors to ≈ 30 Vpk.

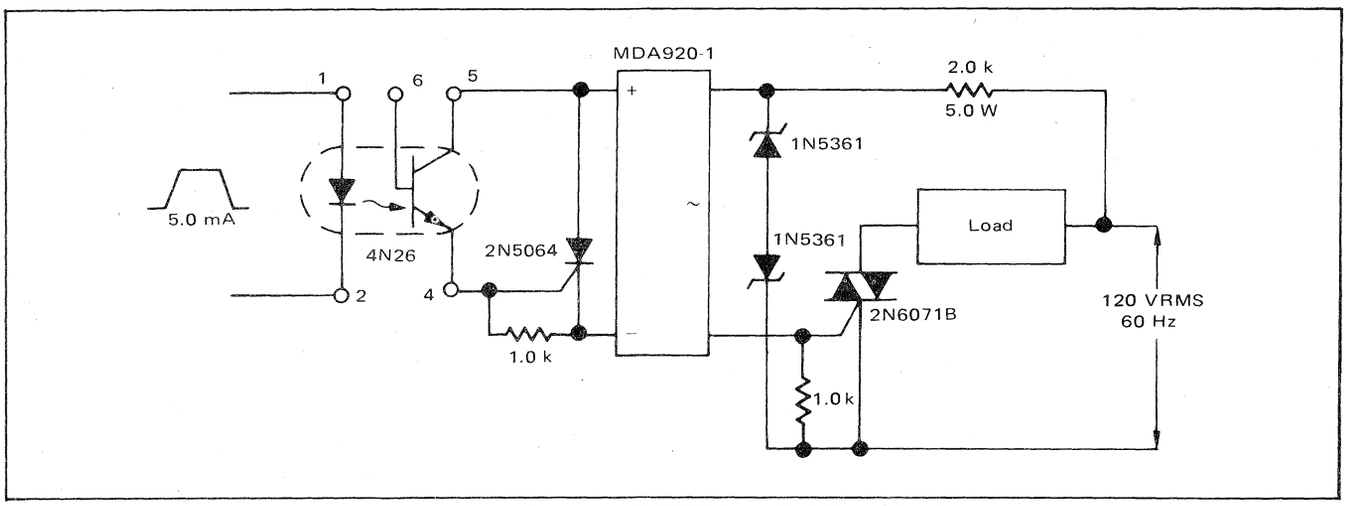


FIGURE 18 – FULL WAVE CONTROL, NORMALLY OFF

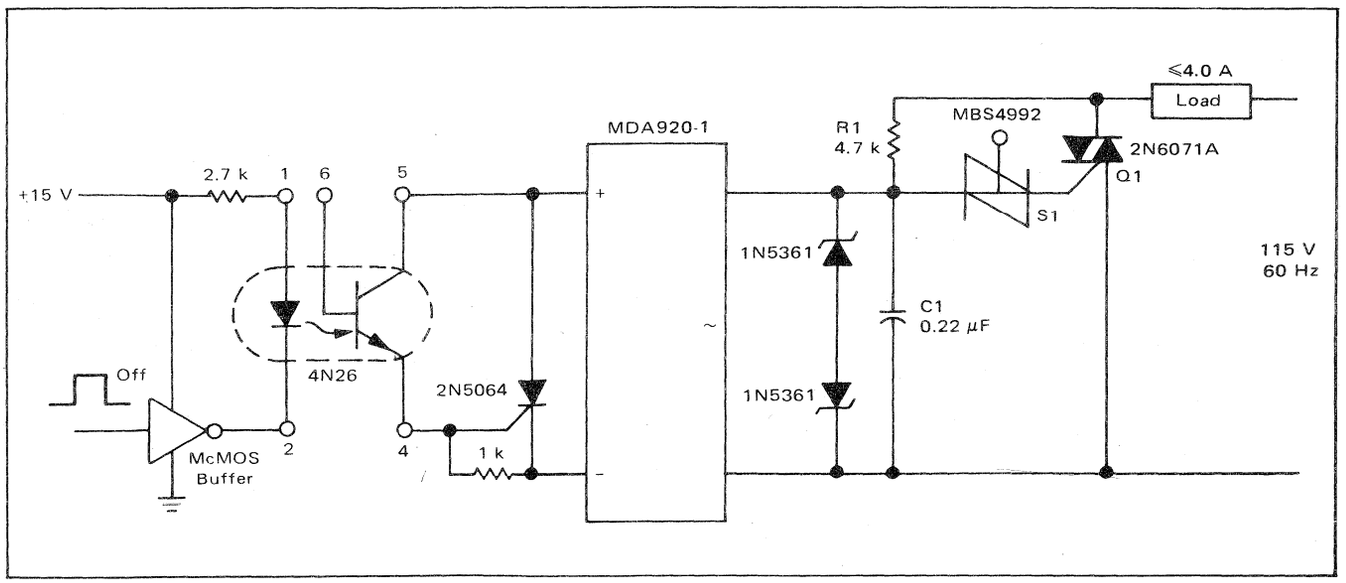


FIGURE 19 – FULL WAVE, ZERO CROSSING CONTROL, NORMALLY OFF

POWER TRANSISTOR CONTROLLED DC LOADS

Industrial logic devices can interface with any power load level, assuming that the circuit has the required number of stable power gain stages. Previous examples described low d.c. power circuits and thyristor controlled a.c. circuits.

By cascading additional power gain stages to the low level examples, higher power loads can be readily driven. The following circuits, Figures 20 through 22, describe the interfacing between industrial logic devices, using both low and high level activation, and a 24V, 18A d.c. motor.

The first example, Figure 20, illustrates low level logic output activation of the motor circuit using McMOS Hex/Buffers. This device, when the output is low, sinks the approximate 8mA base current for the 2N4403 PNP transistor Q_1. This transistor then furnishes base current for the following NPN monolithic 20A darlington 2N6282. Worst case -40°C, 17 A h_{FE} was approximated to be 210 resulting in a base current of approximately 150mA, a value well within the drive capability of transistor Q_1. This current is derived from the +15V logic power supply, which, in some applications, might be excessive.

A circuit that minimizes this drain is shown in Figure 21. It is basically the complement of the previous circuit and employs high level logic output circuit activation. The buffer sources the 8mA base current to the following NPN transistor (2N4401), which in turn sinks the 150mA base current of the complementary Darlington (2N6285). This current is furnished by the +24V motor supply, thus, reducing the drain on the logic supply by this magnitude (≅150mA). For high temperature operation ($T_J \geq 100°C$), the addition of the external base to emitter resistor R_1 across the Darlington input is recommended. This additional leakage current shunt ensures that the device will not go into a thermal runaway condition.

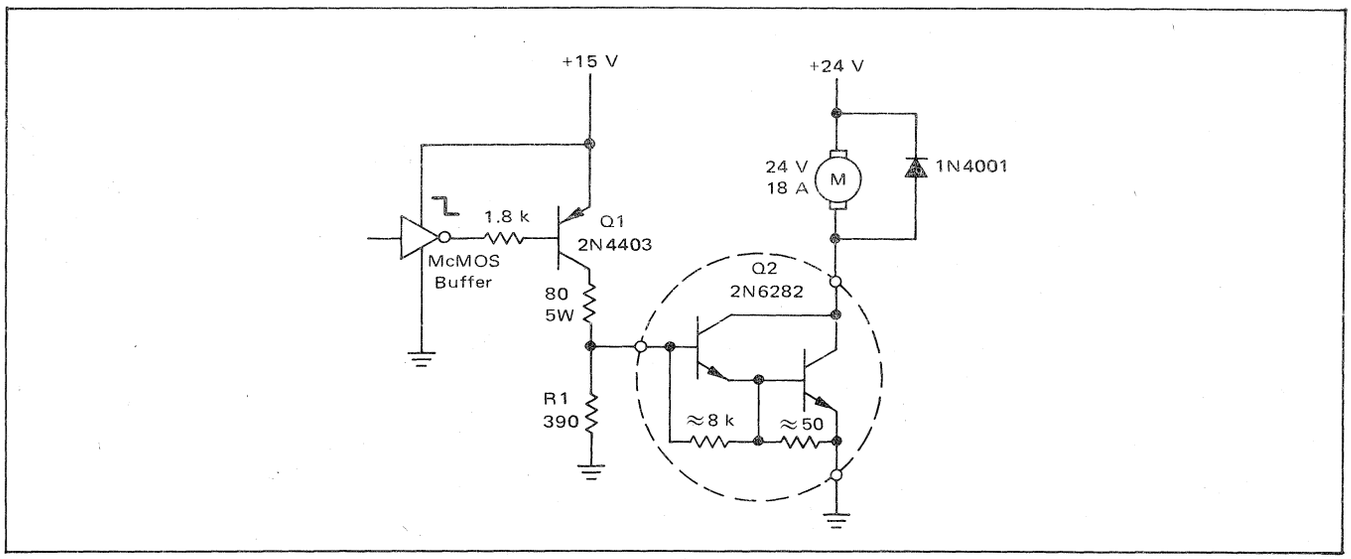


FIGURE 20 – McMOS LOW LEVEL ACTIVATION OF MOTOR LOAD

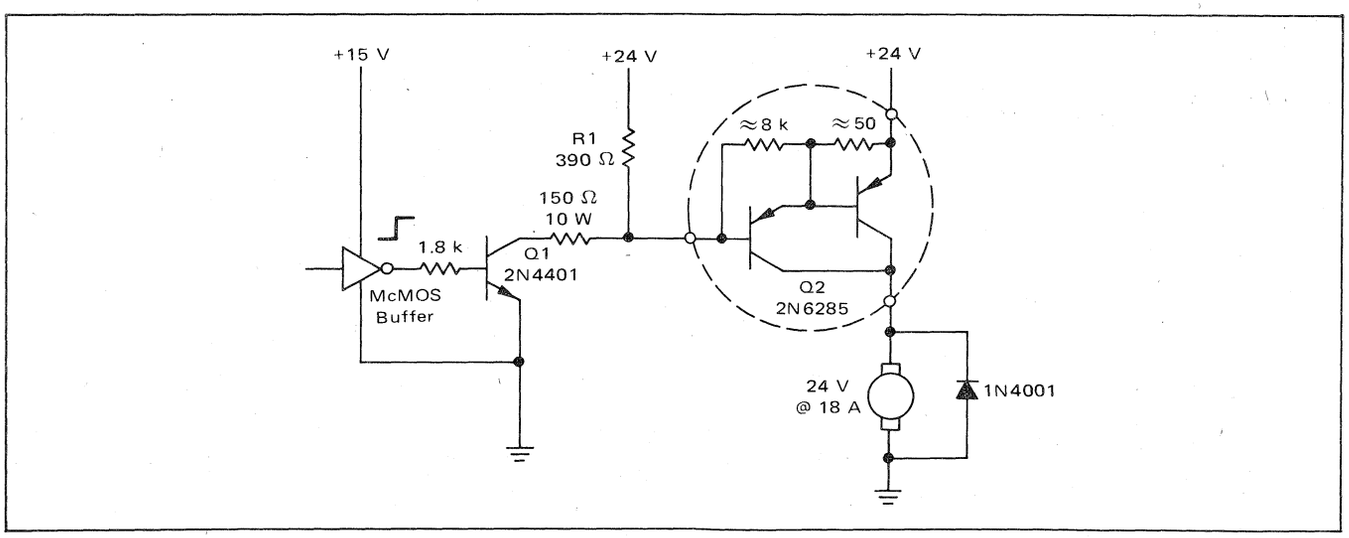


FIGURE 21 – McMOS HIGH LEVEL ACTIVATION OF MOTOR LOAD

The aforementioned circuits supplied Darlington base current through a switched transistor. Another approach is to supply drive current through a pull-up resistor with motor control obtained by means of a transistor clamp across the input of the Darlington, as illustrated in Figure 22. The clamp driver (Figure 22(a)) and clamp (Figure 22(b)) shown for this example are of the MHTL logic family, being respectively a passive pull-up gate and high current driver.

The circuit uses two discrete transistors for the Darlington, the MJE205, 5A plastic case transistor driving the 2N5301, a 30A, TO-3 case device. Their worst case h_{FE}s are 19 and 9 at collector currents of 2 and 18 amps respectively, which thus require an input current of approximately 100mA. When the shunt clamp is de-energized, input current flows, the Darlington saturates and the motor is powered.

The clamp, when energized (motor de-energized), must be able to sink the input current and maintain a saturation voltage less than the ON voltage of the Darlington. The two examples illustrated low level logic activation, Figure 22(a) and high level activation, Figure 22 (b) readily meet these requirements. Diode D_1 is used for high temperature operation to further ensure proper clamping.

CONCLUSIONS

The industrial logic families of McMOS and MHTL can readily interface with power devices when the various blocks are well defined and characterized. Examples of these logic families interfacing with low and relatively high power d.c. and a.c. loads are shown using transistors and thyristors as the load drivers. Such non-linear loads as lamps and d.c. motors are used to illustrate the need for adequate drive current capability of both the logic and the power device. In addition to illustrating the common direct coupled and level translation approach to interfacing, examples of opto-electronic coupling where high isolation is required are also considered and described in detail.

Figure 22a – Passive Pull–Up MHTL
Gate Activation: Low

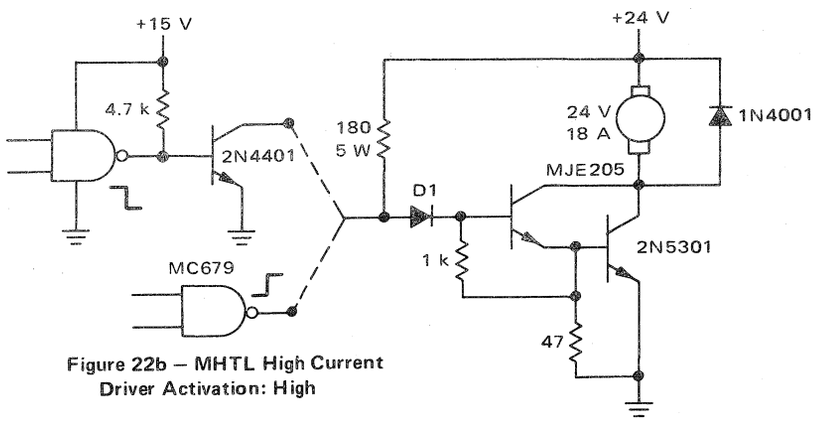


Figure 22b – MHTL High Current
Driver Activation: High

FIGURE 22 – CLAMPED DARLINGTON MOTOR CONTROL

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